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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/332,338	06/14/1999	GUILLERMO J. ROZAS	TRANS11	2806

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EXAMINER	
NGUYEN, DUSTIN	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/332,338	ROZAS ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-52 and 71-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37,38,42-45,49,71,75 and 79* is/are rejected.

7)☐ Claim(s) *39-41,46-58 and 72-78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/31/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 37-52, and 71-79 are presented for examination.

Specification

2. Examiner requests Applicants to update status of any related cases as mentioned in the disclosure [page 19].

Allowable Subject Matter

3. Claims 39-41, 46-48, 50-52, 72-74, and 76-78 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 37, 38, 42, 44, 45, 49, 71, 75, and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohn et al. [US Patent No 5,901,308], in view of Breternitz, Jr. [Us Patent No 5,537,620].

6. As per claim 37, Cohn discloses the invention substantially as claimed including a method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions [Figures 3A-C; and col 3, lines 59-60] comprising:

a first memory operation that involves a first address range [1, Figure 3A; and col 1, lines 53-57];

a second memory operation that involves at least a portion of said first address range [2, Figure 3A; and col 1, lines 57-61]; and

third memory operation intervening said first and second memory operations [3, Figure 3B; and col 5, lines 48-58], wherein it is not known whether said third memory operation involves an address within said first address range [i.e. speculative] [col 2, lines 18-34], wherein at least one of said first through third memory operations comprises a store operation [col 1, lines 27-29]; and

d) determining, during said executing, if said third memory operation involves an address within said first address range [i.e. detect] [col 6, lines 6-col 7, line 10], and if so, raising an exception [col 2, lines 37-43; and col 6, lines 3-15] and re-executing the sequence of instructions including said second memory operation [col 6, lines 35-38].

Cohn does not specifically disclose

b) eliminating said second memory operation from said sequence of instructions;

c) executing said sequence of instructions with said second memory operation eliminated.

Breternitz discloses

b) eliminating said second memory operation from said sequence of instructions [Abstract; and col 1, lines 60-col 2, lines 7];

c) executing said sequence of instructions with said second memory operation eliminated [i.e. eliminate redundant load] [Figure 1; col 8, lines 12-col 9, lines 11].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Cohn and Breternitz because Breternitz's teaching of eliminating instruction would allow to take maximum advantage of the computer architecture and the specific configuration of the individual computer program [Breternitz, col 1, lines 11-15].

7. As per claim 38, Cohn discloses prior to said executing said sequence of instructions, adding information to said third memory operation to allow determination of said first address range [i.e. tag] [col 4, lines 47-50].

8. As per claim 42, Cohn storing a memory address associated with said first address range in a register prior to said executing said sequence of instructions [col 1, lines 52-64; and col 3, lines 22-23].

9. As per claim 44, Cohn does not specifically disclose first and second memory operations would be safely reducible to a single memory operation if said third memory operation were not

intervening. Breternitz discloses first and second memory operations would be safely reducible to a single memory operation if said third memory operation were not intervening [i.e. eliminate redundant] [col 4, lines 59-col 5, lines 5]. It would have been obvious to a person ordinary skill in the art at the time the invention was made to combine the teaching of Cohn and Breternitz because Breternitz's teaching would allow to reduce the processing overhead for improved system performance.

10. As per claim 45, it is rejected for similar reasons as stated above in claim 37. Furthermore, Cohn discloses load and store instructions [col 1, lines 27-29].

11. As per claims 49, 71 and 75, they are rejected for similar reasons as stated above in claim 45.

12. As per claim 79, Cohn does not specifically disclose second store stores back to the first address range the same value that said load instruction loads from the first address range. Breternitz discloses second store stores back to the first address range the same value that said load instruction loads from the first address range [i.e. data dependency] [col 3, lines 17-21]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Cohn and Breternitz because Breternitz's teaching would allow to maintain data integrity.

13. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohn et al. [US Patent No 5,901,308], in view of Breternitz, Jr. [Us Patent No 5,537,620], and further in view of Moreno et al. [US Patent No 5,918,005].

14. As per claim 43, Cohn disclose

said sequence of instructions comprises a fourth memory operation that is in said sequence of instructions after said first memory operation [4, Figure 3A]; and

Cohn and Breternitz do not specifically disclose adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first address range.

Moreno discloses adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first address range [i.e. original order] [col 2, lines 7-40].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Cohn, Breternitz and Moreno because Moreno's teaching would allow to follow program order to prevent system corruption.

15. Applicant's arguments with respect to claims 37-52 and 71-79 have been considered but are moot in view of the new ground(s) of rejection.

16. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for

response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dustin Nguyen
Examiner
Art Unit 2154

VIET D. VU
PRIMARY EXAMINER